

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. .... 09/941,369  
Priority Filing Date ..... August 28, 2001  
Inventor ..... Leonard Forbes  
Assignee ..... Micron Technology, Inc.  
Priority Group Art Unit ..... 2818  
Priority Examiner ..... Viet Q. Nguyen  
Attorney's Docket No. .... MI22-2381  
Title: A Four Terminal Memory Cell, a Two-Transistor SRAM Cell, a SRAM  
Array, a Computer System, a Process for Forming a SRAM Cell, a  
Process for Turning a SRAM Cell OFF, a Process for Writing a SRAM Cell  
and a Process for Reading Data from a SRAM Cell

**INFORMATION DISCLOSURE STATEMENT**

References -- See attached Form PTO-1449


In compliance with 37 C.F.R. §§ 1.56, 1.97, and 1.98, your attention is directed to the references which are listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a continuation application of co-pending application Serial No. 09/941,369, filed August 28, 2001. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned. 37 C.F.R. §1.98(d) and MPEP §609(2). However, copies of the new art cited with this filing are enclosed including references AK, AL, and AN.

Citation of the referenced art is respectfully requested.

Respectfully submitted,

Dated: 8/2/03

By:   
James D. Shaurette  
Reg. No. 39,833

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			ATTY. DOCKET NO. M122-2381		SERIAL NO. Filed Herewith	
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)					APPLICANT Leonard Forbes			
					FILING DATE Filed Herewith		GROUP Unknown	
U.S. PATENT DOCUMENTS								
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate		
	AA	5,285,687	10/1998	Yin				
	AB	5,754,468	5/1998	Hobson				
	AC	6,011,726	1/4/2000	Batson et al.				
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						Yes	No	
	AO	JP2001308298A	11/2001	Hoffman				
	AP	JP410335488A	12/1998	William et al.				
	AO							
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)								
	AR	Lage et al., <i>Advanced SRAM technology - the rate between 4T and 6T cells</i> , "Abstract (Web address - <a href="http://pluto.ei.org">http://pluto.ei.org</a> )						
		Technical Digest - Proceedings of the 1996 IEEE International Electron Devices Meeting Dec. 8-11, 1996.						
	AS	Noda et al., <i>A 1.9-<math>\mu\text{m}^2</math> Loadless CMOS Four-Transistor SRAM Cell in a 0.18-<math>\mu\text{m}</math> Logic Technology</i> , date unknown,						
		ULSI Device Development Laboratories, NEC Corporation, Japan, 5 pages.						
	AT							
EXAMINER				DATE CONSIDERED				
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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	6,184,588	2/2001	Kim et al.			
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FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Subclass	Translation
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